EE 240A Design Project Report

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1. Overview

In this design, folded cascode amplifier was used to achieve high output swing, high bandwidth, and relatively high gain. Then the second stage, consisting of M13 and M16, can help to further improve the gain. M11, in the third branch, is connected with an ideal current source, and is used to build current mirrors. M12, M14, and M19 are used to copy the current to their own branches. M15 is used to bias the gate of M5 and M6, and the bias voltage is 1.25 V. M17 is used to bias the gate of M3 and M4 at 0.55 V, while M18 is used to bias the gate of M7 and M8 at 1.43 V. The schematic with the size of each transistors is shown in Figure 1 below.

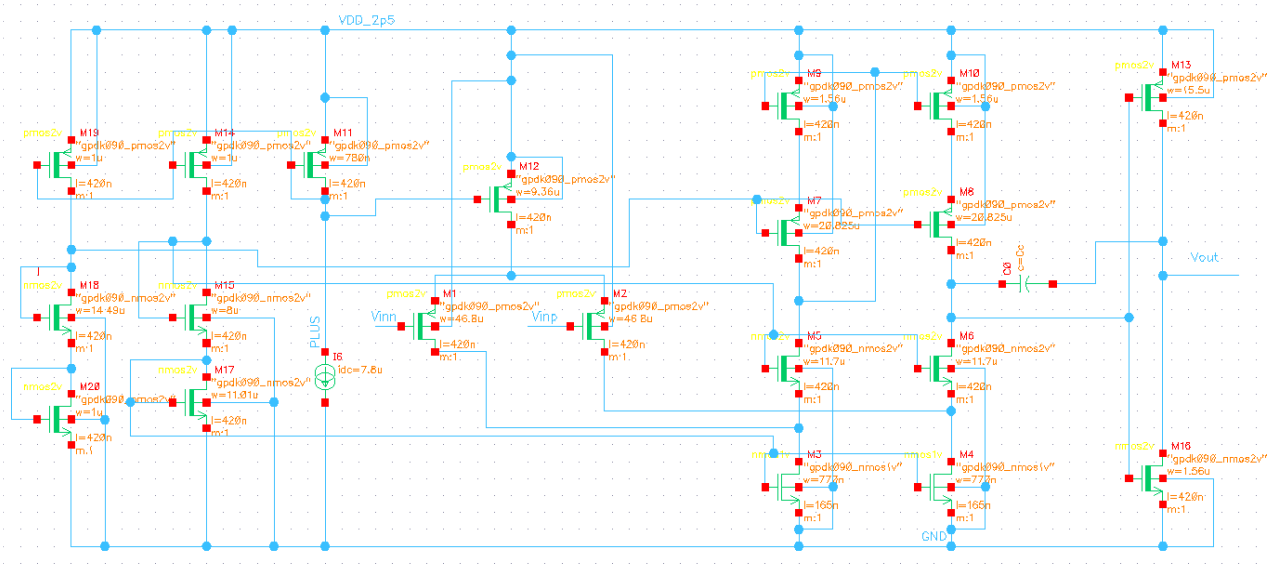

Figure 1. The schematic for the amplifier design, with size labeled near each transistors.

2. Design

First, we need to calculate the open loop gain that we need. From the LCD driver model, we can get the closed-loop gain:

$$A_{CL} = \frac{C_S}{C_F} * \frac{1}{1 + \frac{(C_S + C_F)}{C_F} * \frac{1}{A_{OL}}}$$

where $C_S = 2\ pF$, and $C_F = 1pF$. Therefore, the static error is:

$$\in_{sta} = \frac{3}{A_{DC} + 3}$$

Then we need to use the dynamic error and maximum settling time to determine the position of the dominant pole, p1. The closed-loop gain then becomes:

$$A_{CL} = \frac{C_S}{C_F} * \frac{1}{1 + \frac{(C_S + C_F)}{C_F} * \frac{1 + s/p1}{A_{OL}}}$$

Since the total error is $\in_{sta} + \in_{dyn} = 0.2\%$, and the settling time requirement is:

$$t_{settling} \leq \frac{1}{60 * 272 * 340} = 180.22ns$$

'stepinfo' function in MATLAB (MATLAB code is shown in Appendix) could be used to calculate the settling time with different pole locations. When we split the error equally, that is, $\epsilon_{sta} = 0.1\%$, $\epsilon_{dyn} = 0.1\%$, the design specifications leads to:

$$A_{OL} \geq 2997\ V/V, p1 \geq 7000\ Hz$$

Folded cascode amplifier were chosen in this design, because it could have relatively high gain, very high input/output swing, and also high bandwidth. In my designed circuit, the gain is:

$$A_{OL} = g_{m2} * [(g_{m6} * r_{o6}) * r_{o4} || (g_{m8} * r_{o8}) * r_{o10}] * g_{m16} * (r_{o16} || r_{o13})$$

And the dominant pole is:

$$\omega_{dom} = \frac{1}{[(g_{m6} * r_{o6}) * r_{o4} || (g_{m8} * r_{o8}) * r_{o10}] * g_{m16} * (r_{o16} || r_{o13}) * C_C}$$

Where C_C is the compensation capacitance. From phase 1, we know when Vov is about 0.2V, the speed-power tradeoff is optimized, and when Vov is 0.2V, the $g_m * r_o$ for different devices are plotted. Since we want the gain to be larger than 3000V/V, the length that I chose for both pmos2v and nmos2v transistors are 420nm, and the compensation capacitance should be about 100fF.

Then the width of transistors could be calculated after roughly designing the transconductance and V_{ov}. From phase 1, for nmos2v and pmos2v with length 420nm and width 0.5um, the I_D VS. V_{ov} plot is shown in Figure 2 below. In the preliminary design, the V_{ov} of transistors are all around 0.2V. For example, when the V_{ov} I want is about 0.15V, and the transconductance I determined is 400uS, the drain current I want is then: $I_D = 0.5 g_m * V_{ov} = 30uA$. Therefore, the transistor width should be:

$$W = 0.5um * \frac{30uA}{1.34uA} = 11.2um$$

This width is what I chose for M5 and M6, and the widths of other transistors are also picked through this procedure.

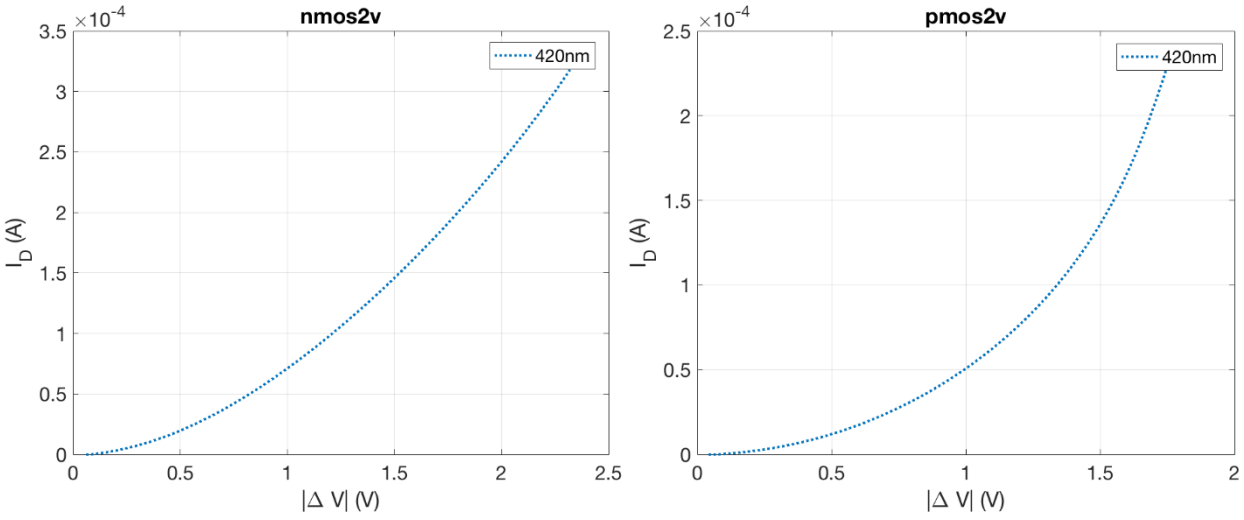

Figure 2. The I_D VS. V_{ov} plot for nmos2v and pmos2v with L=420nm and W=0.5um.

After picking all the transistor sizes, ADE L simulations by Cadence were performed, and based on the simulation results, the widths of each transistor were modified in order to keep all transistors in saturation and all parameters satisfying the specifications.

M3 and M4 are the only two transistors with different length and device type, because the V_{GS} and V_{DS} on them are both always smaller than 1V, and 1v transistors can have better speed-power tradeoff. The length and width design of them also followed the above procedure.

In the preliminary design, the bias voltages are ideal voltage source. Later, when all specifications are met, current mirrors were used to bias the transistors. The first and second branches in my circuit are used for biasing. The current through them are small, because they only provide the bias voltage. M15, M17, and M18 are used for biasing, and M20 is actually not for biasing. M20 is used for helping M18 to provide 1.43V voltage. Because the current through M18 is small, without M20, the V_{GS} of M18 is 1.43V, and the width of it would be too small, leading settling time increase.

3. Transistor and Bias Summary

Table 1 below lists the type, dimension, drain bias current, gate-to-source voltage, transconductance, and also output conductance of each transistor.

Table 1. The parameter list of all transistors.

Transistor	Type	Length(nm)	Width(um)	I_D(uA)	$\lvert V_{gs}\rvert$(mV)	g_m(uS)	g_{ds}(uS)
M1	pmos2v, 1st stage	420	46.8	42.1117	661.919	807.914	18.3153
M2	pmos2v, 1st stage	420	46.8	42.1117	661.919	807.914	18.3153
M3	nmos1v, 1st stage	165	0.77	71.2486	549.862	357.938	37.8397
M4	nmos1v, 1st stage	165	0.77	71.2486	549.862	357.938	37.8397
M5	nmos2v, 1st stage	420	11.7	29.1374	722.252	446.143	19.8074
M6	nmos2v, 1st stage	420	11.7	29.1374	722.252	446.143	19.8074
M7	pmos2v, 1st stage	420	20.825	29.1374	714.909	465.771	11.3479
M8	pmos2v, 1st stage	420	20.825	29.1374	714.909	465.771	11.3479
M9	pmos2v, 1st stage	420	1.56	29.1374	955.141	125.846	10.4618
M10	pmos2v, 1st stage	420	1.56	29.1374	955.141	125.846	10.4618
M11	pmos2v, current source	420	0.78	7.8	817.176	48.2917	1.43003
M12	pmos2v, current mirror	420	9.36	84.2225	817.176	539.343	22.8426
M13	pmos2v, 2nd stage	420	15.5	308.335	955.141	1354.55	47.2717
M14	pmos2v, current mirror	420	1	10.7756	817.176	64.9634	1.87205
M15	nmos2v, bias	420	8	10.7756	703.174	195.608	8.6933
M16	nmos2v, 2nd stage	420	1.56	308.335	1544.86	518.581	27.3102
M17	nmos2v, bias	420	11.01	10.7756	549.862	204.15	7.68759
M18	nmos2v, bias	420	14.49	10.4448	710.148	217.956	10.0258
M19	pmos2v, current mirror	420	1	10.4448	817.176	63.7264	1.84771
M20	nmos2v, help bias	420	1	10.4448	720.897	83.3154	3.54847

4. Layout

The layout of my designed circuit is shown in Figure 3 below. In order to match all transistors well, I split the finger width so that I will have almost the same number of fingers per stack. The transistor names and width are shown in the layout. My design process is: split the transistor size to several fingers, and make sure each finger length is smaller than 5um. Then identify the transistors that could be placed on the same stack. After splitting, some transistor widths were changed a little, but this will not hurt the performance of the entire circuit. The number of fingers per stack is about 22. There are 4 p-channel stacks and 4 n-channel stacks, and the matched transistors are connected using interdigitation method. Approximately, the area that my design take is:

$$A = 20um * 18.9um = 379um^2$$

In order to match the transistors, the wiring will then be a little bit complex. Besides, the two nmos1v transistors make the layout seem slightly inconsistent.

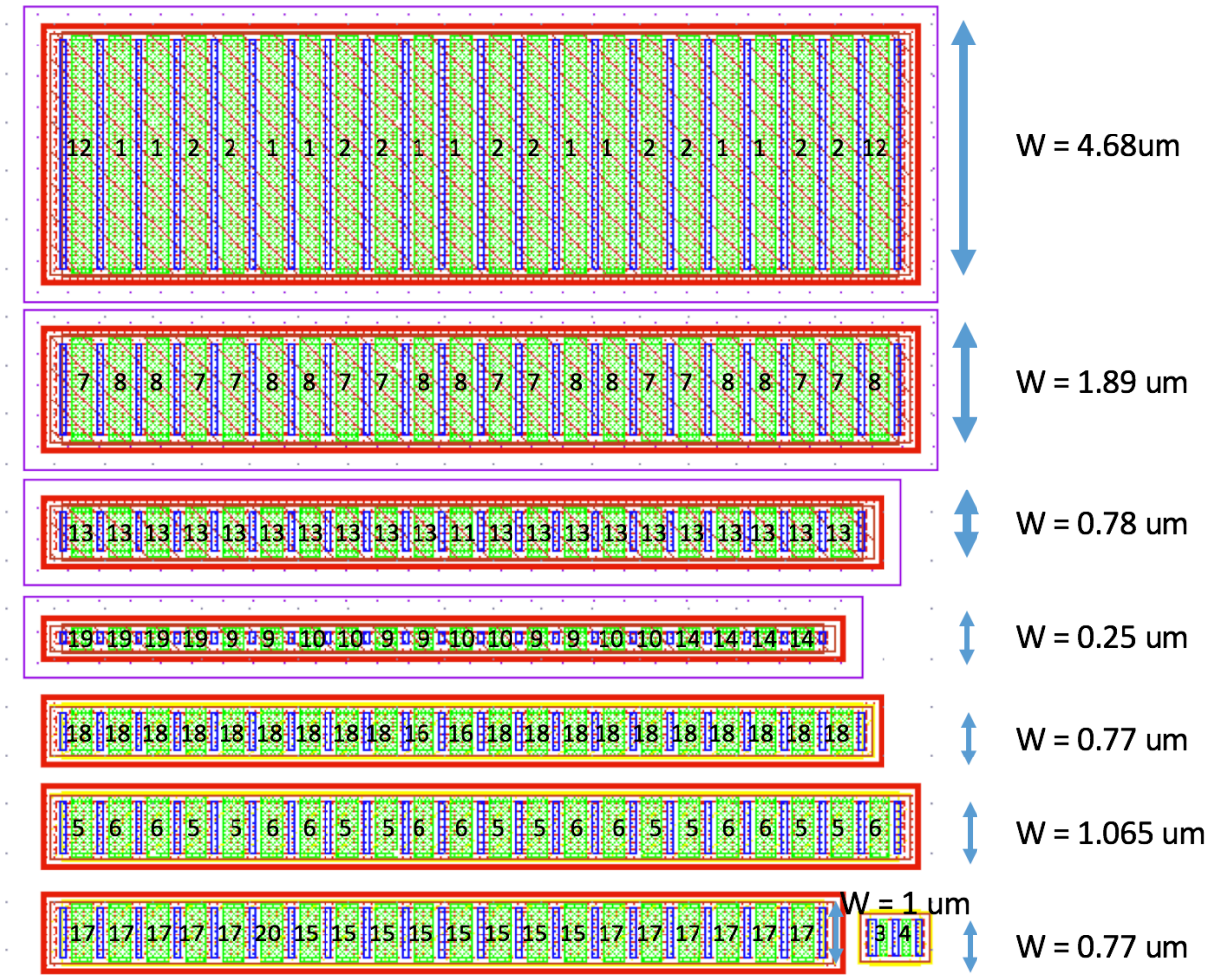

Figure 3. The layout of the amplifier. Only transistors without wiring are shown.

5. Discussion

5.1 The Simulation Results

Firstly, the AC testbench was performed to verify the gain, stability, CMRR, and PSRR all meet the requirements. Figure 4 below shows the cm_gain, ps_gain, dm_gain, PSRR, and CMRR vs. frequency. As we can see, $A_{OL} = 9178\,V/V$, which means the static error is about 0.0327%, and the dynamic error could be about 0.1673%. Besides, bandwidth is about 100kHz, which means my dominant pole is larger than 7kHz, as calculated in section 2. Also, the CMRR and PSRR in DC can be both calculated below and viewed in Figure 4, which imply the CMRR and PSRR meet the requirements.

$$CMRR = \frac{dm_{gain}}{cm_{gain}} = 5545.99\frac{V}{V} = 74.8796dB$$

$$PSRR = \frac{dm_{gain}}{ps_{gain}} = 1069.85\frac{V}{V} = 60.5865dB$$

$$BW = 100kHz$$

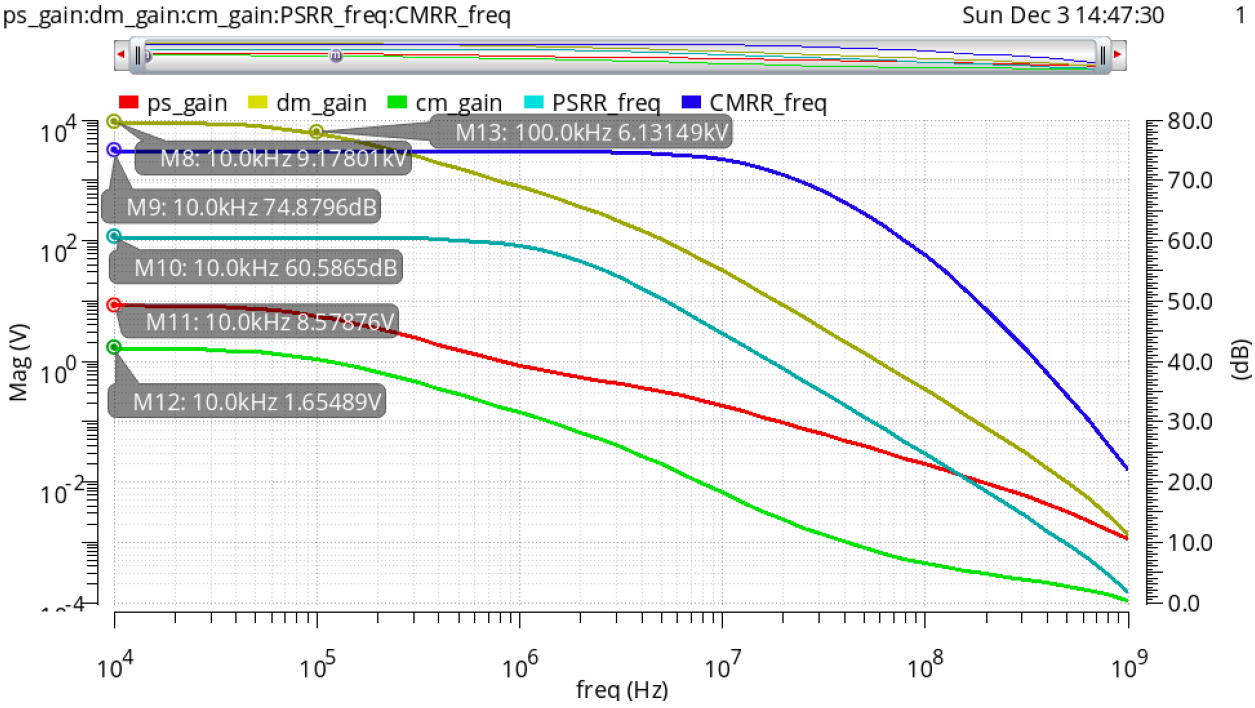

Figure 4. The plot for ps_gain, dm_gain, cm_gain, PSRR and CMRR VS. frequency.

Figure 5 below shows the bode plot of the loop gain in my design. As we can see, when the magnitude of loop gain is 0dB, the phase of the loop gain is about 60°. Therefore, the phase margin is about 60°, larger than what in the specification: 35°.

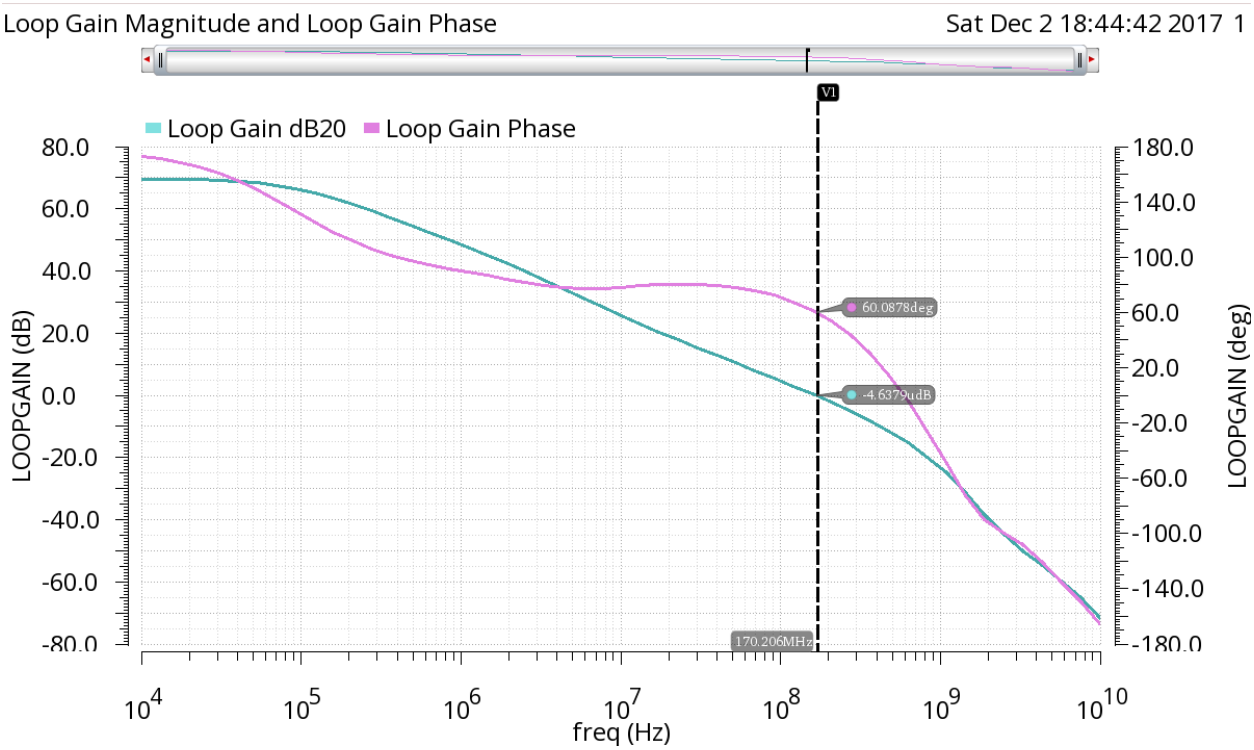

Figure 5. Bode plot of loop gain.

Then transient testbench was then performed to analyze the power consumption, settling time, and output swing of my circuit. Figure 6 shows the transient response when the input is 1V and the output is 2V. It is obvious that the output swing is $\geq 2V$. Besides, since the output is settled at 1.45784V, the lower bound for rising edge when the error is within 0.2% is 2.45384V, and the settling time is:

$$t_{RisingSettling,1V} = 2.57958us - 2.4us = 179.58ns$$

Similarly, the upper bound for the falling edge when error is within 0.2% is 0.46184V, and the falling settling time is about:

$$t_{FallingSettling,1V} = 1.57729us - 1.4us = 177.29ns$$

As for the power consumption, Figure 7 shows the current vs. time plot. We can roughly get the power consumption by multiplying the average of the quiescent current with the power supply, that is:

$$Power_{1V} = \frac{321.508uA + 425.336uA}{2} * 2.5V = 933.555uW$$

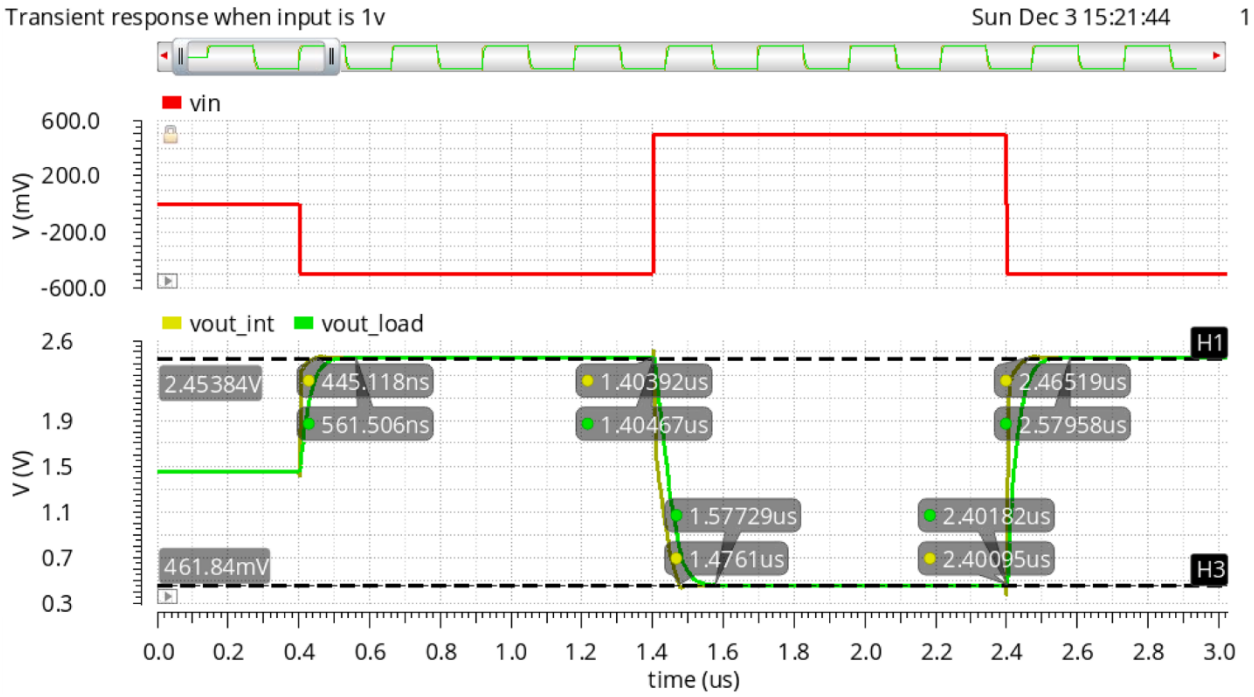

Figure 6. The transient response when the input is 1V. The settling time for both rising edge and falling edge can be derived in this plot.

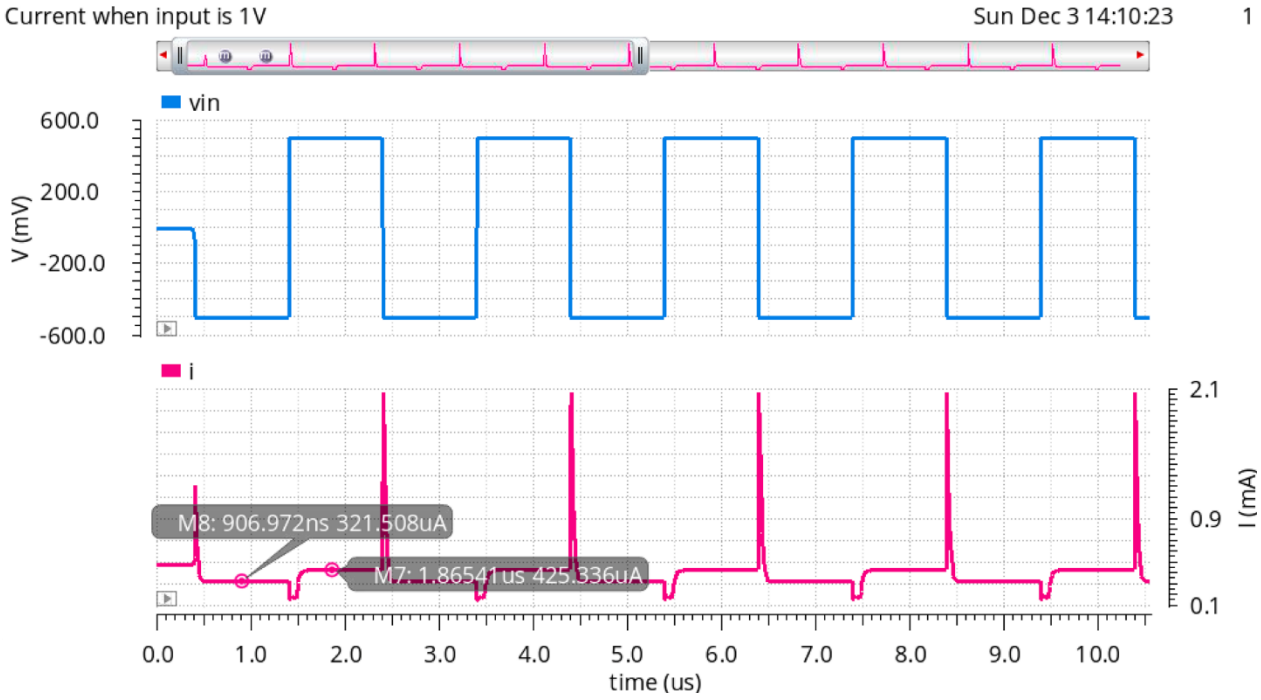

Figure 7. The current vs. time plot when the input is 1V. The power consumption can be roughly calculated based on the average current and power supply.

When the input is 10mV and the output is 20mV, similar analysis was performed. Figure 8 shows the corresponding transient response. Since the output was settled at 501.102mV, the lower bound for rising edge when the error is within 0.2% is 511.062mV, and the settling time is:

$$t_{RisingSettling,10mV} = 2.50973us - 2.4us = 109.73ns$$

Similarly, the upper bound for the falling edge when error is within 0.2% is 491.142mV, and the falling settling time is about:

$$t_{FallingSettling,10mV} = 1.51476us - 1.4us = 114.76ns$$

As for the power consumption, Figure 9 shows the current vs. time plot. We can roughly get the power consumption by multiplying the average of the quiescent current with the power supply, that is:

$$Power_{10mV} = \frac{353.373uA + 350.054uA}{2} * 2.5V = 879.234uW$$

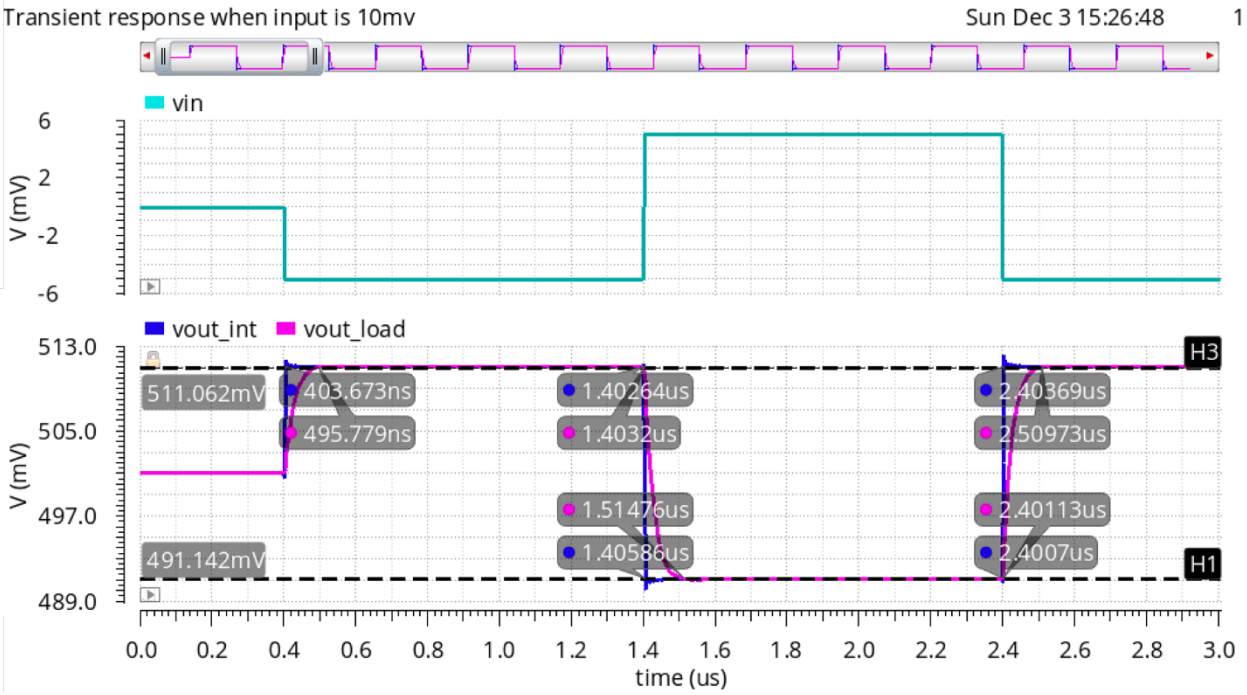

Figure 8. The transient response when the input is 10mV. The settling time for both rising edge and falling edge can be derived in this plot.

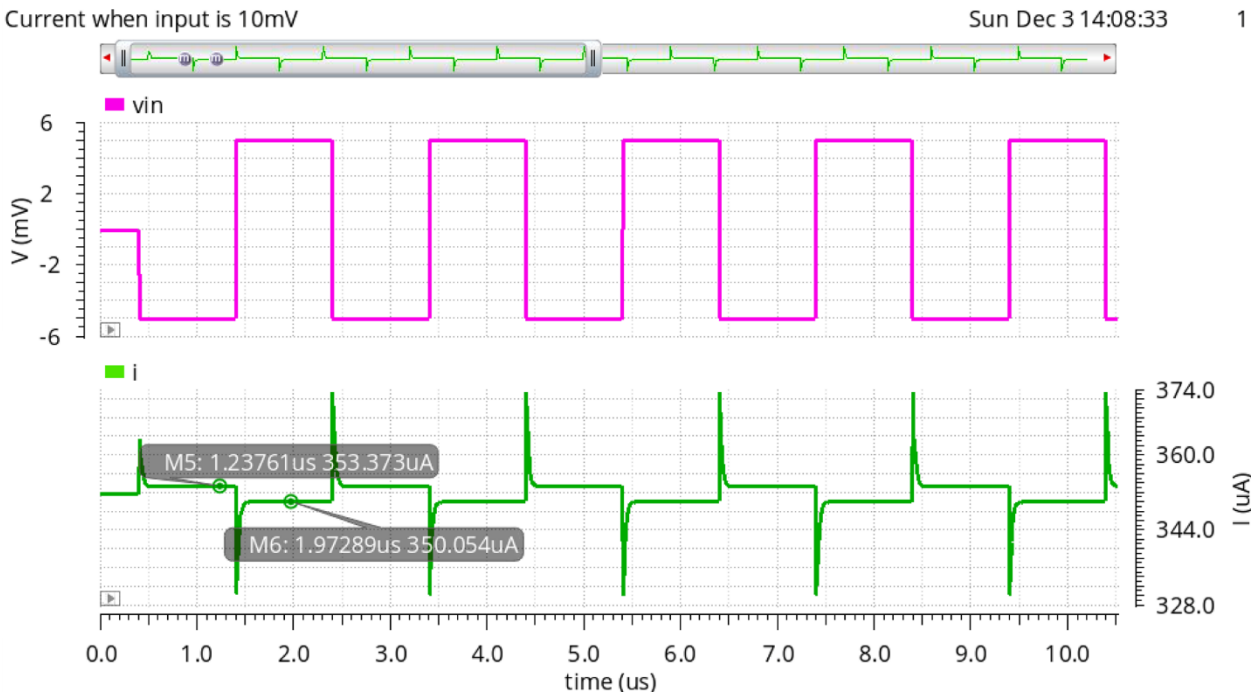

Figure 9. The current vs. time plot when the input is 10mV. The power consumption can be roughly calculated based on the average current and power supply.

The testbenches that provided by instructors can also measure the above parameters, power consumption and settling time, directly. The results of the ADE L simulation are shown in Table 2 below. All the parameters are close to the numbers that were derived from the plots above, and it is obvious that my design can meet the requirements very well.

Besides, the compensation capacitance I used is 100fF, which is very small comparing with the maximum total capacitance requirement. Furthermore, the maximum current mirror ratio is the current ratio through M12 and M11. The ratio is calculated below, and also satisfied the requirement.

$$\text{Maximum current mirror ratio} = \frac{I_{DM12}}{I_{DM11}} = \frac{84.2225uA}{7.8uA} = 10.80$$

Table 2. The comparison between the design specifications and the simulated performance of my design. The design can meet all the specifications very well.

Parameters	Specifications	Design			
		For 1V input		For 10mV input	
Settling Time	≤ 180.22 ns	rising	falling	rising	falling
		179.581 ns	177.163ns	109.456ns	115.245ns
Power Consumption	≤ 1.00 mW	0.938131mW		0.879293mW	
Figure of Merit to Maximize	$\frac{10^{-9}}{T_{settling} * P_{total}}$	5.94		9.87	
Power Supplies	0V, 1.2V, 2.5V	0V, 2.5V			
Closed Loop DC Gain	2	2			
Total Error	≤ 0.2%	≤ 0.2%			

Output Voltage Swing	≥ 2 V	≥ 2V
Maximum Current Mirror Ratio	20	10.8
Maximum Total Capacitance	25 pF	100 fF
CMRR at DC	≥ 60 dB	74.8796 dB
PSRR at DC	≥ 60 dB	60.5865 dB
Phase Margin	≥ 35°	60.2394°

5.2 The Unique Attempts in My Design

During the design process, although the V_{ov} of all transistors were initially set to 0.2V, modifications need to be done. For example, as for M1 and M2, their g_m is related to the open loop gain, and we need to increase the width to make g_m larger. Therefore, their V_{ov} is smaller than 0.2V.

As for the compensation capacitance, a Cadence sweep was performed, and it turns out that a 100fF capacitance is good enough to make the circuit function stably, which also confirms that the hand calculated capacitance value is reasonable.

Besides, during my design, the ideal current source was set to k*10uA, and the width of all transistors are k*W, where W are the widths that can make the amplifier work well initially. In order to adjust the settling time and power consumption easily, the constant k was swept by Cadence. Therefore, when k is 0.78, that is, the ideal current source is 7.8uA and the width of all transistors are multiplied by 0.78, the power consumption and settling time can all meet the specification very well.

The output stage is also crucial in the design. At first, I used a class A output stage, that is, a pmos2v transistor was used to mirror the current source, and a nmos2v transistor was used as a common source amplifier. However, the current through this branch is very large. When I noticed the gate voltage of the pmos and nmos in the output stage are actually very close, I tied the output directly to both gates. The power consumption of this branch decreases a little bit, and the requirements can be met. However, the drain current through this branch is still huge: 308.335uA, making this branch consume about 80% of the total power in my circuit. This is because the V_{GS} is relatively fixed, and if the W/L of the two transistors are too small, the speed will be significantly hurt. Therefore, the current through this branch is very large. I tried to use a source follower as a level shifter to reduce the V_{GS} of both M13 and M16 to 0.7V, but then the PSRR is reduced to 59dB, and the falling edge is not sharp because the current is not enough. Therefore, I still used this design, but it is worth to point out that the second stage in my circuit really hurt the power consumption, and further improvement is needed.

Next, M3 and M4 in my circuit are nmos1v. I made this modification because for M3 and M4, their r_o is related to the gain, and the open loop gain of my circuit is very high (larger than 12,000V/V). Although nmos2v devices with L=420nm can have larger r_o, nmos1v devices with L=165nm is much faster. Therefore, in order to let my settling time meet the requirement under the same V_{ov}, I used nmos1v devices for both M3 and M4, although this made my open loop gain decrease to 9178V/V.

Finally, as stated before, the M20 in my circuit does not have biasing task. It is only used to ensure the gate voltage of M18 is 1.43V while the V_{GS} of M18 is relatively small under very small current.

6. Conclusion

In this project, I designed a 2-stage folded cascode amplifier. This amplifier has very large open loop gain: 9178V/V, relatively high bandwidth: 100kHz, large phase margin: 60°, high PSRR: 60dB, and very high CMRR: 75dB. Besides, when put this amplifier in the feedback loop, the output swing is larger than 2V, while the settling time when the input is 1V and the tolerated error is 0.2% is 179.581ns, which is smaller than the requirement: 180.22ns. Furthermore, the power consumed in the circuit is 938.131uW. The main drawback of my design is that the output stage consumes a huge amount of power, and further improvement is needed, in order to improve the figure of merit.

During this design, I learned how to design a real amplifier based on what I have learned in the entire semester. This project requires the knowledge of current mirror, differential amplifiers, frequency analysis, stability analysis, op amplifier specifications, output stage, and also layout & mismatch. After the design, I know how to transform the specifications to the amplifier level specification, design a preliminary amplifier and then modify the transistor parameters. Besides, I learned in the design, what parameters are the most important ones and what parameters can be ignored in the starting point. This design project helped me to combine all the knowledge together and then apply what I have learned in the lecture to real design process. Also, this project deepens my understanding about trade-off.

The phase 1 is really helpful in the design, because from that, I know the optimal V_{ov} for the given transistors are 0.2V, and the transistor length that fits my design is about 420nm. Based on that, the width of all transistors can be easily picked. The iteration in the design to make the amplifier really function well is challenging but also interesting. This design project is time-consuming, but also makes me realize that this is what research is and what engineers always do.

Professor Muller explained the project clearly in the lecture, and the GSIs are super helpful in debugging the circuit. However, I think if there are more explanations and design examples, it would make the project easier for us. Because when the project is posted, it is very hard to start. If the instructors could provide a sample design process, even it is a very simple circuit, that could help a lot.

7. Appendix: MATLAB Code

```
clear; clc;
close all;
tmin = 1/(60*272*340);
Cs = 2e-12;
Cf = 1e-12;
tVal = linspace(0,1e-7,10000000);
err = 0.002;

%parameters that needs to be changed:
for p1 = 1e3:1e3:50e3

    wp1 = 2*pi*p1;

    e_sta = err*.5;
    e_dyn = err - e_sta;

    %calculate the gain
    A = ((1-e_sta)/e_sta)*(Cs+Cf)/Cf;
    s = tf('s');
    f = 1/2;
    OL = A/(1+s/wp1);

    CL = (Cs/Cf)/(1+(Cs+Cf)/(OL*Cf));
    A_sta = (Cs/Cf)/(1+(Cs+Cf)/(A*Cf));

    %spec analysis

    [Gm,Pm,Wgm,Wpm] = margin(OL);
    info = stepinfo(CL,'SettlingTimeThreshold',e_dyn,tVal,A_sta);
    if info.SettlingTime < tmin
        pole = p1;
        break
    end

end
fprintf('The open loop gain is %f, and the dominant pole is %f Hz\n',A,pole);
```