EE230B Final Project: Comparison of Bulk and SOI FinFETs (May. 2018)

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***Abstract*—In this work, 10nm technology node bulk and SOI NMOS FinFET transistors are designed and simulated to meet low power requirements using Sentaurus three dimensional TCAD simulator. The tradeoffs between bulk and SOI FinFETs, including electrical and thermal characteristics, are compared and explained.**

***Index Terms*—Low power applications, Bulk FinFET, SOI (silicon-on-insulator) FinFET, Short Channel Effects, Self-heating.**

I. Introduction

FINFET has replaced the position of conventional single-gate MOSFET in semiconductor industry during the scaling-down, because it can significantly reduce the short channel effects by its better gate controllability over the channel. There are two types of FinFETs in terms of substrate: one is fabricated on silicon-on-insulator (SOI) substrates, and one is bulk FinFET, which is similar with the standard bulk CMOS fabrication technology.

In this report, 10 nm technology node FinFETs for low power applications in both SOI and bulk technologies are designed to meet the specifications from the 2015 ITRS[1]. The design details, as well as the device characteristic differences and tradeoffs between SOI and bulk FinFETs, will be analyzed.

II. Design decisions and device structures

In the FinFETs design, the most important parameters that determine the device performances are channel doping, source/drain doping, and dielectric thickness. Here, constant doping profile is used, to mainly focus on the differences between bulk and SOI FinFETs. The channel doping should be low, because lower doping concentration in channel can give higher carrier mobility, and also eliminate discrete dopant fluctuation effects on the threshold voltage. The doping level at source and drain sites should be high enough to reduce the series resistance. As for the gate dielectric thickness, it should be small to provide smaller subthreshold swing, but not super small, because otherwise the tunneling will happen. After determine the doping levels and dielectric dimensions, the work function of the gate metal needs to be tuned to meet the threshold voltage requirement.

During the design process, subthreshold swing requirement is the first to be considered, and the SOI FinFET is the first structure to be designed. The subthreshold swing needs to be about 70 mV/dec. After dope $1\times10^{11}cm^{-3}$ Boron in the channel and $1\times10^{20}cm^{-3}$ Arsenate in the source and drain, as well as use HfO_2 as the gate dielectric material and set it to be 3 nm, the first simulation was performed. The subthreshold swing in this case is about 74 mV/dec, which means our initial design is reasonable but still needs more optimizations. Then the thickness of the gate dielectric was set to be 2.8 nm, while kept the other parameters unchanged, and the simulation result turned out to have 72.5 mV/dec subthreshold swing. Then the source/drain doping concentrations were decreased to $5\times10^{19}cm^{-3}$ and $1\times10^{19}cm^{-3}$ to see whether better subthreshold swing would be got, because the larger doping concentration would result in larger electric field at the drain-channel junction, and then result in larger drain capacitance. The large drain capacitance can also degrade our subthreshold swing. Therefore, the subthreshold swings for $5\times10^{19}cm^{-3}$ and $1\times10^{19}cm^{-3}$ source/drain doping are 71.8 mV/dec and

68.3 mV/dec, respectively. Then the work function of the gate metal is swept from 4.4 to 4.7 eV, and 4.58 eV turned out to be the one that sets the threshold voltage at 336mV. This work function is reasonable, because there are a lot of metals have this work function, such as Ag, Cu, Mo, Sb, W[2] ,etc.

Then the bulk FinFET was designed. Except for keeping the same channel, source, drain doping concentrations, and the gate dielectric thickness, bulk doping concentration also needs to be carefully considered. If the doping concentration is too low, punchthrough will happen in the bulk, which means there will be a path for source/drain leakage current, and gate would have less control over I_D. Therefore, the slope of $\log I_D$ vs V_G should be flatter, and the leakage current will be huge. However, if the bulk concentration is too high, the electric field and junction capacitance at the drain-bulk junction are large, which will result in large junction leakage and also junction breakdown. Therefore, in this simulation, after sweeping several bulk concentration numbers, $1\times10^{17}cm^{-3}$ boron is chosen to be doped in the bulk to give better device performance. Then work function of the gate metal was tuned to 4.57eV to keep the threshold voltage still at 336mV.

The structure of the half SOI FinFET is shown in Figure 1(a), and its doping profile is shown in Figure 1(b). The bulk FinFET half structure is shown in Figure 1(c), with its doping profile in Figure 1(d). The structure figures are without Si, in order to show the gate dielectric and gate matal more clearly.

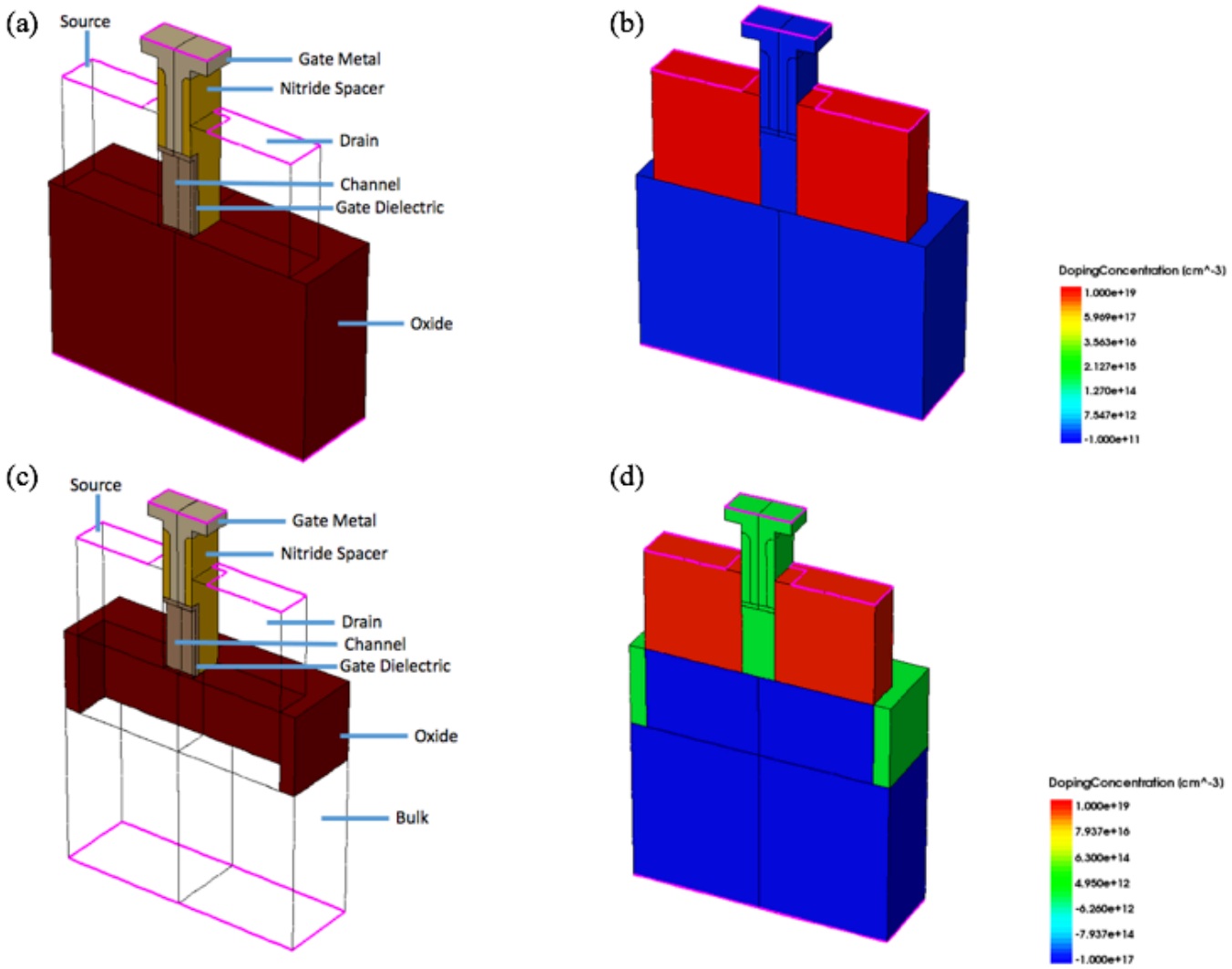


Figure 1. The half structure of (a) SOI FinFET and (c) bulk FinFET without Si, and doping profile of (b) SOI FinFET and (d) bulk FinFET

The fabrication process of the two types of FinFETs should be easy, because we are using constant doping profiles. The standard recipes could be used. Figure 2 shows the main differences between SOI and bulk FinFET fabrication[3]. After defining the fins, gate will be deposited and well-etched, and then source and drain can get implanted.

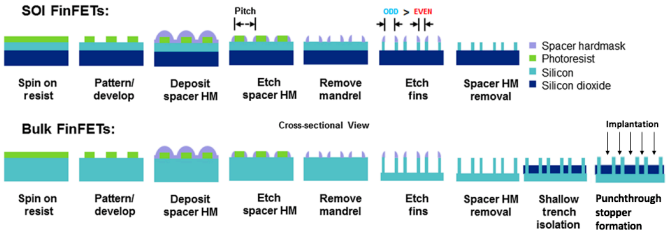


Figure 2. The process for fin self-aligned double patterning lithography scheme for SOI and bulk FinFETs

The designed parameters of the FinFETs are summarized in Table 1 below.

Table 1. The summary of the dimensions, doping profiles, and metal work function of designed FinFETs.

Dielectric thickness (nm)	2.8	
Gate length (nm)	20	
Fin width (nm)	6	
Fin height (nm)	42	
Channel length (nm)	90	
Channel doping (cm^{-3})	1×10^{11}	
Source/Drain doping (cm^{-3})	1×10^{19}	
Bulk doping (cm^{-3})	1×10^{17} (only for bulk FinFET)	
Metal work function (eV)	SOI FinFET	Bulk FinFET
	4.58	4.57

III. Simulation Results

The gate voltage was swept from 0V to Vdd (0.75V) while keeping V_{DS} at both Vdd (saturation region) and 0.05V (linear region), to see the device performances in the subthreshold region. Figure 3 shows the logI_D vs. V_{GS} curves for both SOI and bulk FinFET. Subthreshold swing, DIBL (drain induced barrier lowering), leakage current, and on current can be calculated based on this plot, and the results are shown in Table 2.

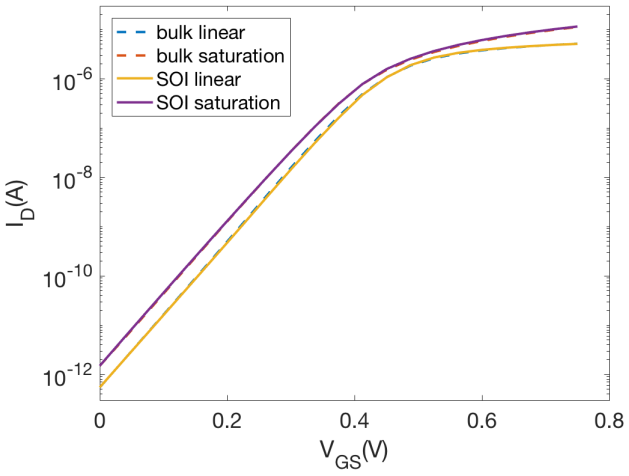
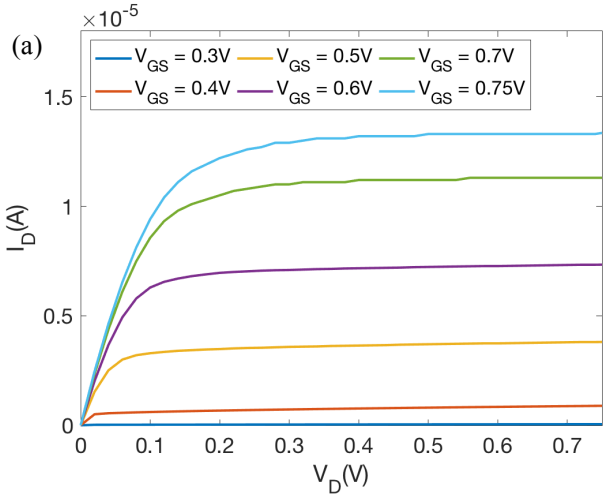


Figure 3. The logI_D vs V_{GS} curves for both SOI and bulk FinFET at both linear and saturation regions

Table 2. Comparison of ITRS requirements and simulation results for SOI and bulk FinFETs.

FinFET type	Requirement	SOI	Bulk
Subthreshold Swing (mV/dec)	70	68.295	67.888
DIBL (mV/V)	/	34.67	31.53
Ion (uA)	637	13.3	12.7
Ioff (pA)	100	1.51	1.50
Ion/Ioff	6.37×10^{6}	8.807×10^{6}	8.467×10^{6}
V_{Tsat} (mV)	336	336	336

Figure 4 below shows I_D-V_D relationships for $0 \le V_D \le$ Vdd at V_{GS} = 0.3V, 0.4V, 0.5V, 0.6V, 0.7V and 0.75V, for both SOI FinFET at 3(a), and bulk FinFET at 3(b). When V_{GS} = 0.3V, both devices are not on because the V_{GS} is even smaller than the threshold voltage. For other V_{GS}, from the simulation results, we can extract saturation drain current I_{Dsat} (when V_{DS} = Vdd) at different V_{GS} (shown in Table 3) and analyze their relations.



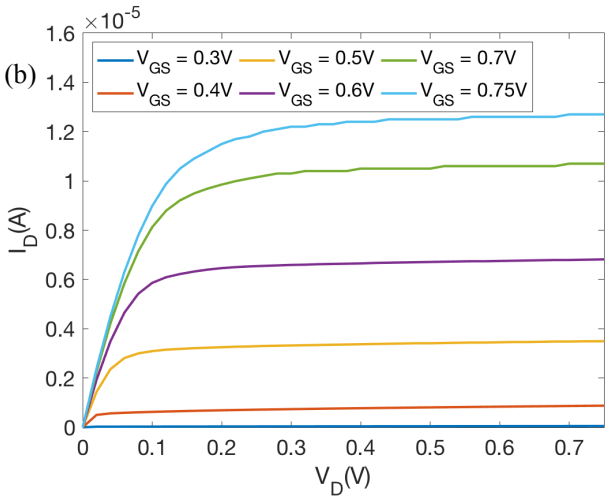


Figure 4. The I_D vs V_D curves for (a) SOI and (b) bulk FinFET at V_{GS} = 0.3V, 0.4V, 0.5V, 0.6V, 0.7V, and 0.75V

Table 3. Extracted I_{Dsat} vs V_{GS} simulation data for both SOI and bulk FinFETs.

V_{GS} (V)	0.4	0.5	0.6	0.7	0.75
SOI FinFET I_{Dsat} (mA)	0.90	3.81	7.34	11.3	13.3
Bulk FinFET I_{Dsat} (mA)	0.88	3.50	6.82	10.7	12.7

By plotting I_{Dsat} vs V_{GS} simulation results (shown in Figure 5), we can see that there is a quite linear dependence of I_{Dsat} on V_{GS} instead of a square-law dependence. A least squares linear fitting for SOI FinFET gives the linear dependence equation I_{Dsat} = (35.84 mA/V) × V_{GS} – 13.72 mA, with a fitting coefficient r^2=0.996, and for bulk FinFET, I_{Dsat} = (34.22 mA/V) × V_{GS} – 13.19 mA, with a fitting coefficient r^2=0.994. Both indicate good linear dependences.

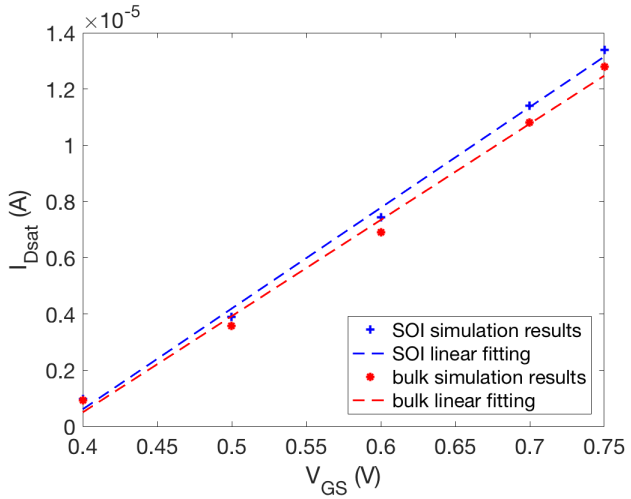


Figure 5. Linear dependence of drain saturation current on gate voltage

The temperature profiles when V_{GS} = V_{DS} = Vdd are also simulated for SOI and bulk FinFETs, as shown in Figure 6. The thermal contacts are at the contact of substrate, gate, source, and drain, and the boundary temperature is 300K. It is obvious that the temperature in the SOI channel is much higher than that in the bulk FinFET channel. Figure 7 shows the maximum temperature in the two FinFETs under different bias conditions, and this can also prove that the temperature in bulk is much lower than that in the SOI FinFET.

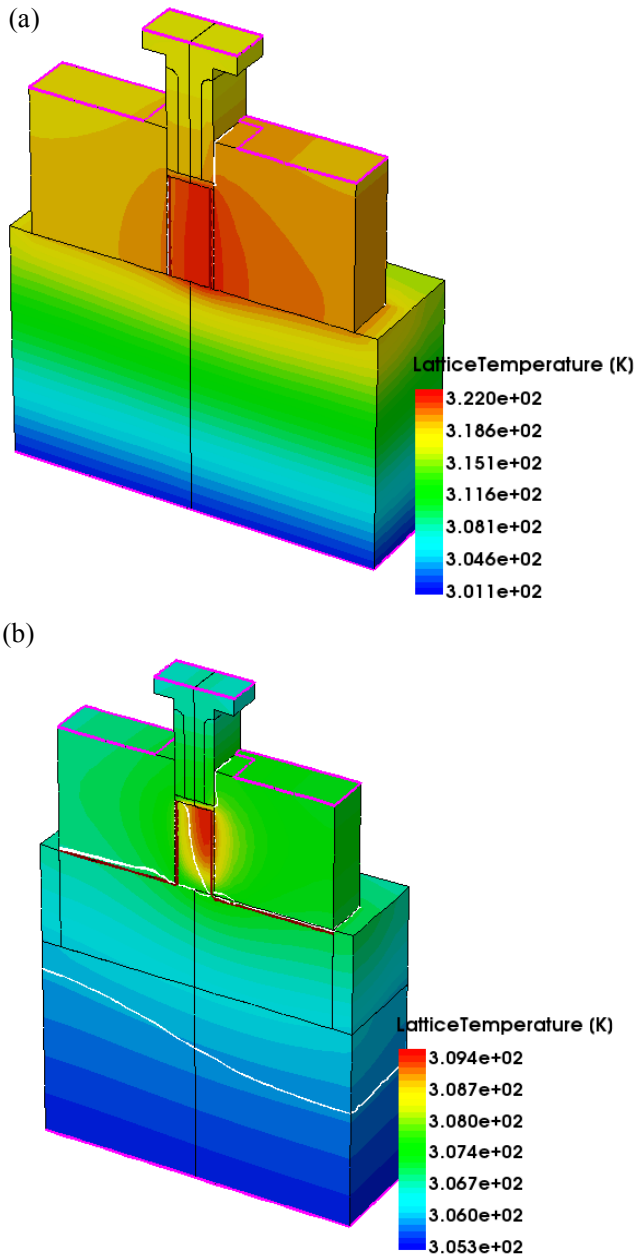


Figure 6. The temperature profile of (a) SOI FinFET and (b) bulk FinFET when V_{GS} = V_{DS} = Vdd

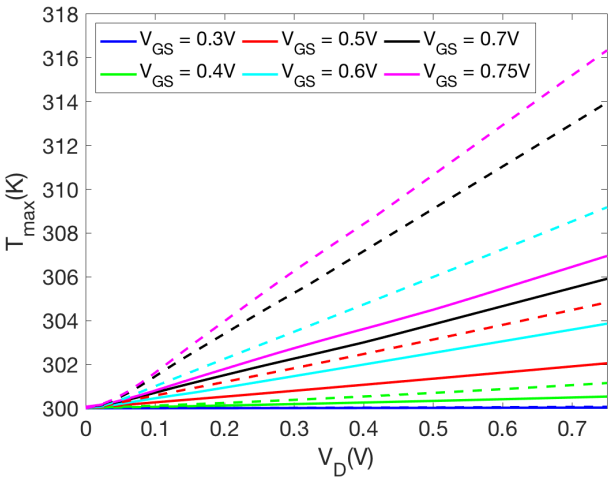


Figure 7. The maximum temperature SOI FinFET (dashed line) and bulk FinFET (solid line)

IV. Discussion

First, from the logI_D vs. V_{GS} curves, SOI and bulk FinFETs have very close performances in terms of subthreshold swing, DIBL, off leakage current, and on current.

When sweeping the drain voltage on different gate voltages, both SOI and bulk FinFETs have nearly constant drain current. After extracting the saturation drain current and plot with different gate voltages, linear relationships between saturation drain current and gate voltage are shown for both SOI and bulk FinFETs. This can be explained by velocity saturation of short channel device. When V_D = 0.75V, the electric field profiles of the channel, for both SOI FinFET and bulk FinFET, are shown in Figure 8 below. Since the saturation velocity happens when the electric field is about 10^5 V/cm, it is obvious that the fields in both two types of FinFETs are high enough to reach velocity saturation of electron drift. When velocity saturation happens, I_{Dsat} is linearly proportional to (V_{GS}-V_T) instead of a square-law dependence for long channel device. The simulation results clearly show this linear dependence.

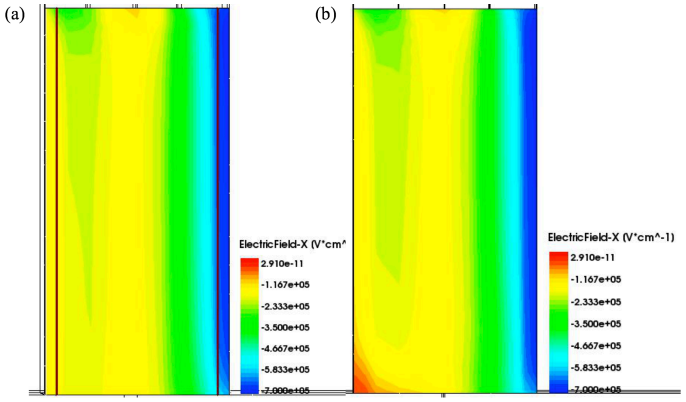


Figure 8. The electric profile in the channel of (a) SOI FinFET and (b) bulk FinFET when V_{GS} = V_{DS} = Vdd

The temperature profiles of both FinFETs indicate that bulk FinFET has much less self-heating than SOI. This is because Si has more than 100 times higher thermal conductivity than SiO_2[4]. Therefore, the SOI substrate prevents heat dissipation, making the temperature in SOI FinFET much higher than that in the bulk FinFET. The rising operating temperature can degrade the carrier mobility, which then decreases the drain current. Beside, the high operating temperature also causes reliability issues.

Since the channel of both FinFETs are near intrinsic, no obvious floating body effects were seen. Besides, from I_D-V_D curves of SOI FinFET and bulk FinFET, SOI has slightly larger current than bulk FinFET. Figure 9 shows the electron mobility of both FinFETs. The mobility of them are very close. Therefore, the lower current in bulk is because the series resistance of bulk is larger than that of SOI FinFET.

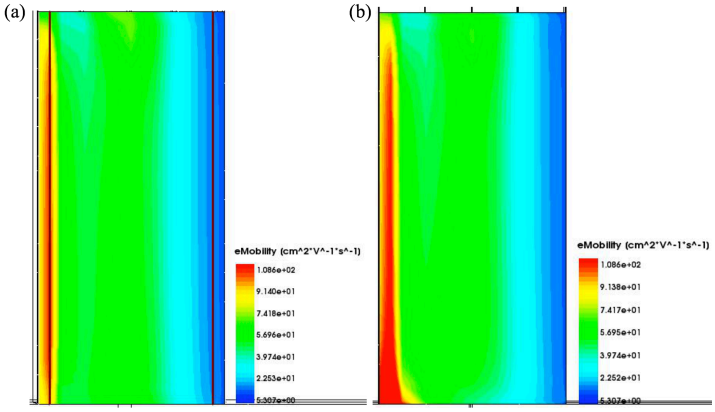


Figure 9. The mobility profile in the channel of (a) SOI FinFET and (b) bulk FinFET when V_{GS} = V_{DS} = Vdd

Except for the above electrical properties differences, there are other tradeoffs need to be considered. For example, SOI FinFET is much easier to fabricate. From Figure 2 above, shallow trench isolation (STI) needs to be grown for bulk FinFET in order to separate the channel in each device, and multiple doping steps are required, because the doping concentrations in the bulk are different from those in the channel to prevent punchthrough. Besides, the fin shape and height are more difficult to control in the bulk FinFET. The fin shape in SOI is often rectangular, while in bulk is always tapered because of the STI process[5]. The tapered fin has worse V_T roll-off, because the wider fin base has worse electrostatic control than the top, and the current density is not uniform along the fin height[6].

V. Conclusion

Both SOI FinFET and bulk FinFET have great gate control over the channel, which can be seen from the low subthreshold swing and DIBL, and their performances are about the same. Besides, both type of FinFETs have linear relationships between the drain saturation current and the gate voltage, which is caused by the velocity saturation inside the channel. SOI FinFET has less series resistance because its drain current is larger than bulk under the same circumstances. SOI has more self-heating than bulk, because heat cannot dissipate from the substrate as well as the bulk FinFET, and this may cause performance and reliability problems. However, SOI FinFET has much easier fabrication process and well-controlled fin shape, although the SOI substrate is more expensive and has more defect density[7]. Therefore, if easier fabrication process of bulk FinFET can be developed, and rectangular fin shape can be built, bulk FinFET will be more attractive to use in the future.

References

[1] International Technology Roadmap for Semiconductors 2.0, 2015 Edition.

[2] John R. Rumble. CRC Handbook of Chemistry and Physics version 2008, p. 12–114.

[3] A. Yagishita, “Process and Device Technologies for FinFET and Its Alternative Devices,” IEEE SOI Conference Short Course, Foster City, CA, October, 2009.

[4] Kleiner, M., Kuhn, S., & Weber, W. (1996). Thermal conductivity measurements of thin silicon dioxide films in integrated circuits. *IEEE Transactions on Electron Devices,43*(9), 1602-1609. doi:10.1109/16.535354

[5] T. Hook, “FinFET Isolation Approaches and Ramifications: Bulk vs. SOI,” FDSOI Workshop at Hsinchu, Taiwan, April, 2013.

[6] B. Cheng, A. R. Brown, X. Wang and A. Asenov, "Statistical Variability Study of a 10nm Gate Length SOI FinFET Device," in *Proc. IEEE Silicon Nanoelectronics Workshop*, Honolulu HI USA, June 10-11, 2012, pp. 69–70.

[7] Lee, J. (2015). Bulk FinFETs: Design at 14 nm Node and Key Characteristics. *Nano Devices and Circuit Techniques for Low-Energy Applications and Energy Harvesting KAIST Research Series,*33-64. doi:10.1007/978-94-017-9990-4_2